A HIGH PERFORMANCE TRANSCEIVER CHIPSET FOR MILLIMETER-WAVE COMMERCIAL DIGITAL COMMUNICATION SYSTEMS

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ABSTRACT

A high performance Q-band monolithic HEMT transceiver chipset has been developed for millimeter-wave commercial digital radio systems. This highly compact transceiver chipset consists of low noise amplifier, power amplifier with detector, voltage controlled oscillator with buffer amplifier, mixer and harmonic mixer. The chipset has demonstrated high yield making it suitable for high volume commercial applications.

INTRODUCTION

Microwave radios in 38 GHz frequency band can provide reliable short haul point-to-point links in applications such as personal communication network (PCN) and other cellular radio network base station links. This application is actively being pursued by European as well US microwave industry since the availability of the frequency spectrum between 35 and 40 GHz provides reliable and cost effective communication link [1].

Most of the transceiver chipset development to this date has been concentrated at lower microwave frequencies for wireless applications such as wireless LAN, PBX and other data collection applications [2,3]. In this paper, we shall present, for the first time, a compact and high performance transceiver chipset at Q-band for commercial microwave digital radio applications. This transceiver chipset was developed for Continental Microwave Technology Limited, a major manufacturer of microwave radio equipment and meets their stringent performance specifications.

PROCESS

One of the major challenges in the development of this chipset was to achieve low noise figure, low phase noise as well as high power performance from the same process technology. To that end, we have utilized TRW's highly reliable and manufacturable 0.15 μm InGaAs/AlGaAs/GaAs pseudomorphic HEMT fabrication technology. This process has been engineered to have a high breakdown voltage and high current densities. To improve the breakdown voltage, the GaAs cap layer is optimized and the AlGaAs layer is left undoped and the Schottky gate is recessed to this undoped region. To increase the current density, an additional planar doping is employed to increase the amount of charge in the 2-dimensional electron gas. The device optimization was performed to ensure high aspect ratio, that is high ratio of gate length to the gate to channel separation. This enables the device to provide low noise, high gain, high efficiency as well as high cutoff frequency for millimeter wave operation. Typically, for a 0.15 μm x 320 μm device, gate to drain voltage of 9 volts, maximum channel current of 500 ma/mm, and f_T greater than 75 GHz is obtained. The process is capable of providing both low noise as well as power performance consistently.

CHIPSET DESIGN

The transceiver chipset consists of a low noise amplifier, power amplifier, voltage controlled oscillator, mixer as well as harmonic mixer in a typical system architecture shown in Fig. 1.

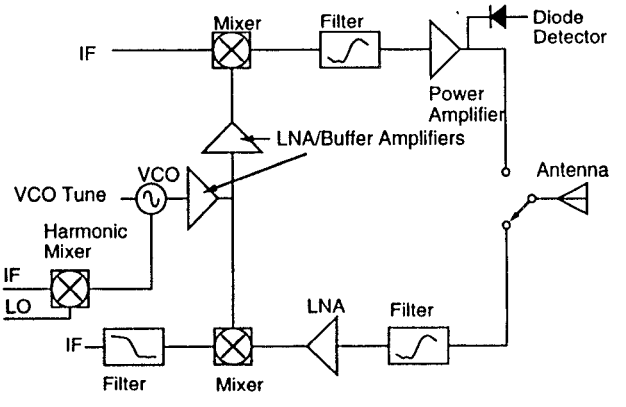

Fig. 1 Functional block diagram of a 35-40 GHz transceiver for PCN applications.

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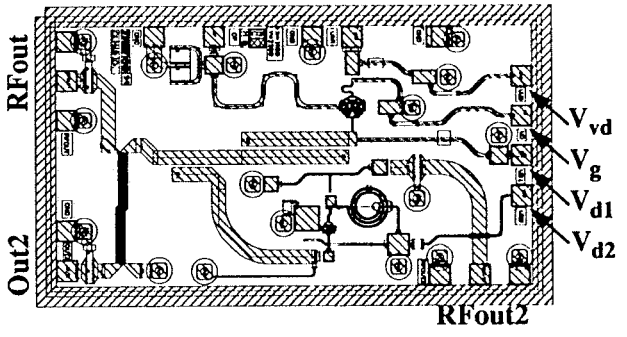
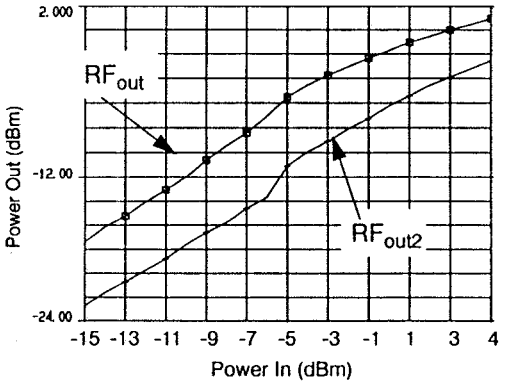
The voltage controlled oscillator provides signals for the synthesizer and LO drive. As shown in Fig. 2, the VCO chip (size 1.4 mm x 2.5 mm) consists of several ports. It utilizes a common source FET configuration and a distributed resonator to provide positive return loss over the desired tuning range. Additionally, a self-biased buffer amplifier and Lange coupler were integrated onto the chip in order to provide multiple outputs. The main VCO output is split using a Lange coupler to provide LO power to the mixers in both the transmit and receive paths. The output power is also sampled and amplified to provide sufficient power to the harmonic mixer which is needed for phase locking. A port is also provided for an off-chip varactor tuning diode. The measured impedance at the varactor port shows negative resistance region starts from 29 GHz. The VCO can be tuned from 35 to 37 GHz by varying the control tuning voltage from 0 to 5 volts with 4 dBm of output power. The isolation between output ports is better than 30 dB. Initial measured phase noise is consistently better than -98 dBc/Hz at 1 MHz offset in this frequency range. As a comparison, previously published results in this frequency range show that MESFET VCO achieved -85 dBc/Hz at 1 MHz offset (greater than 300 MHz tuning range at 32 GHz) [4,5] and HBT VCO achieved -107 dBc/Hz at 1 MHz offset (about 1 GHz tuning bandwidth at 35, 37 and 40 GHz) [6].

The low noise amplifier is used in the receiver front end and also as a general purpose gain amplifier. For overall superior performance, a two stage, balanced topology has been incorporated. Series feedback in the first stage provides unconditional stability while shunt feedback in the output stage ensures flat gain. The balanced configuration doubles the output power and at the same time provides better input and output match. As shown in Fig. 3, it provides wide band operation from 22 to 42 GHz. This chip has 11 dB gain and less than 5 dB noise figure. The return loss at both input and output ports is better than 15 dB. The measured power at 37 GHz is greater than 15 dBm at 1 dB compression point. Both positive and negative power supply are required to bias this chip which operates at 5 volts. The chip size is 1.4 mm x 2.5 mm. This performance is comparable to that published in [7].

Fig. 4 shows the mixer is used both as an upconverter in the transmit path and as a downconverter in the receive path. The RF and LO of this single balanced mixer operate over 35 to 40

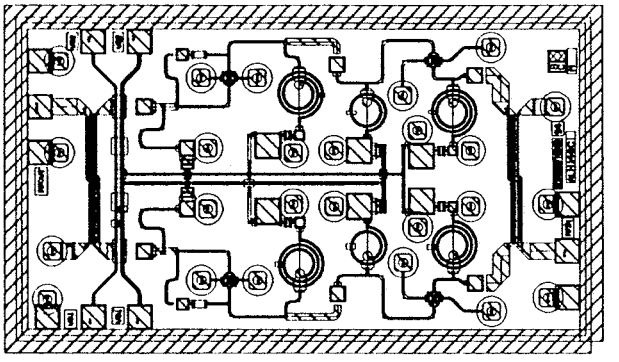


(a)



(b)

Fig. 2 Voltage controlled oscillator (a) layout and (b) measured output power at output port (RFout) and coupled output port (RFout2) versus input power at the varactor port, frequency =35 GHz.



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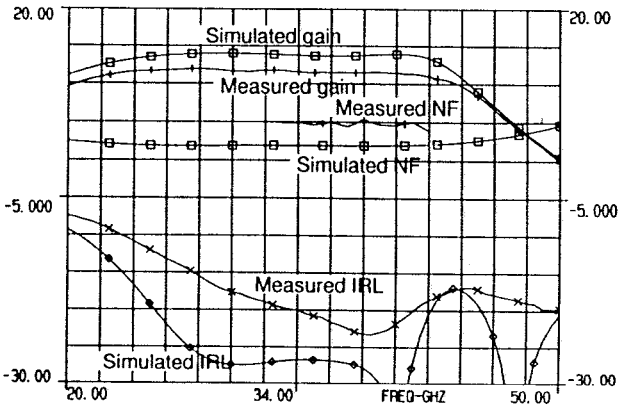
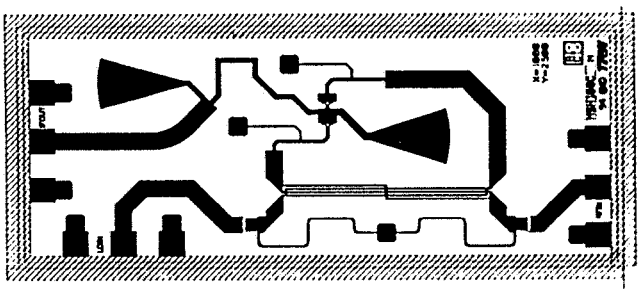


(b)

Fig. 3 Low noise amplifier/buffer amplifier (a) layout and (b) simulated and measured gain, noise figure, input and output return loss as a function of frequency.



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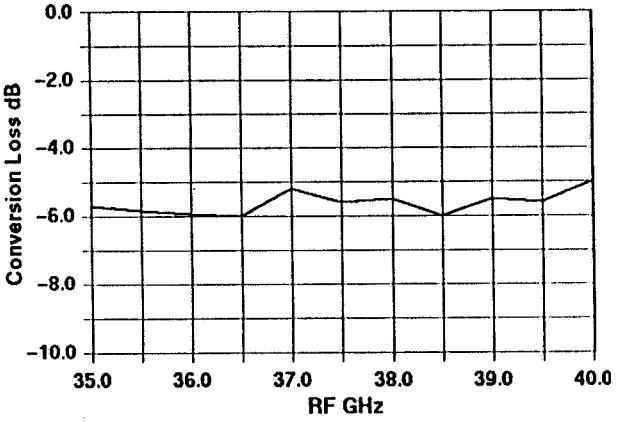

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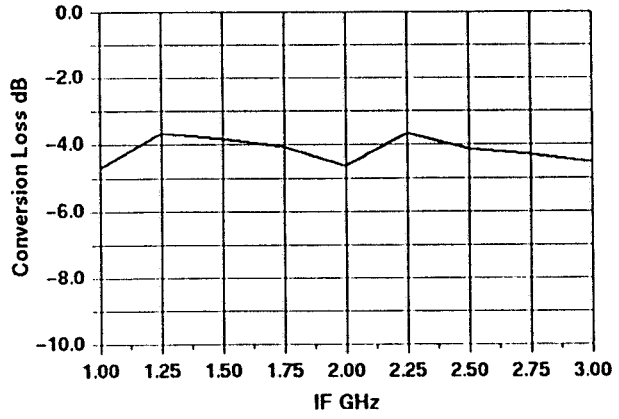
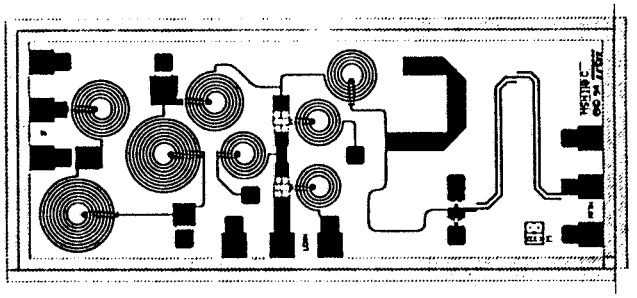
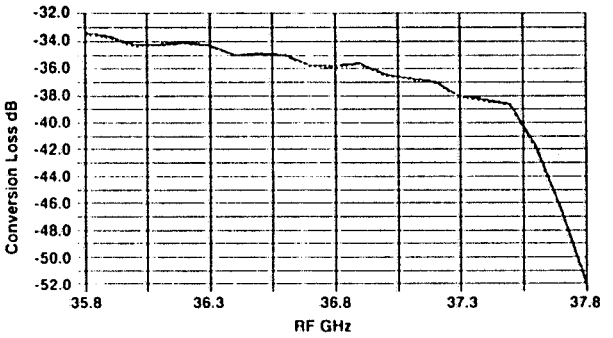


(c)

Fig. 4 Single balanced mixer (a) layout, (b) conversion loss as a downconverter at P_{LO}=11 dBm, F_{IF}=2 GHz (c) conversion loss as an upconverter with P_{LO}=11 dBm and F_{LO}=36.5 GHz.



(a)



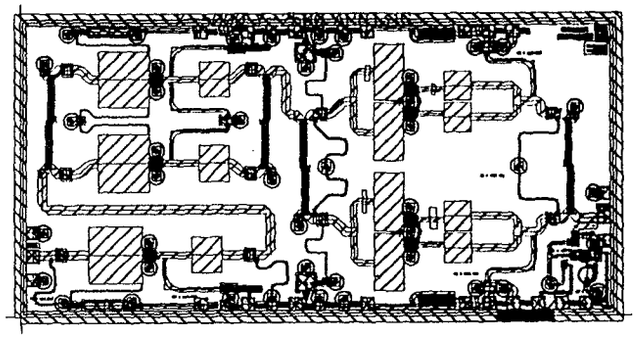
(b)

Fig. 5 Harmonic mixer (a) layout (b) conversion loss FIF=FRF-16*FLO.

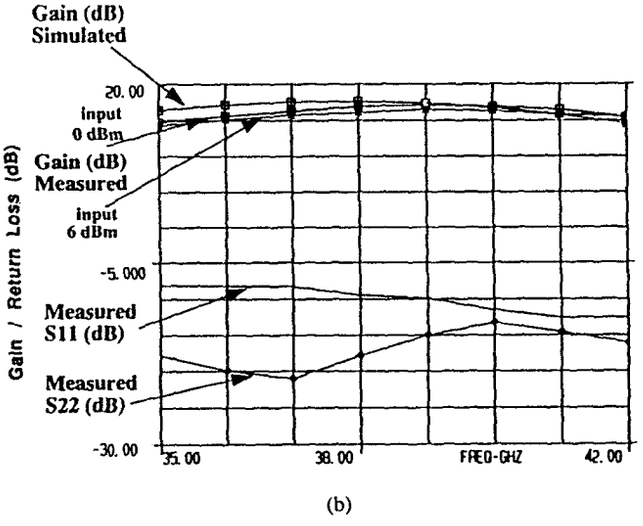
GHz and provides IF output in the frequency range of 1 to 3 GHz. The 180° hybrid is realized with a Lange coupler and an additional 90° line. The mixer uses 4 finger, 36 µm diodes. The conversion loss of this mixer is 8 dB as a downconverter and is 6 dB as an upconverter at an LO power level of 11 dBm. The return loss of this mixer, measured as a downconverter, was better than 15 dB at the RF port and better than 8 dB at the IF port. The chip size is 1 mm x 2.5 mm.

The harmonic mixer (Fig. 5) downconverts the VCO frequency using a S-band local oscillator to provide an IF signal which is used for phase locking of synthesizer. It is implemented for the first time as a monolithic circuit and provides state-of-the-art performance. This mixer uses 4 finger, 28 µm diodes, edge coupled RF filter, and a lumped element IF and LO diplexer circuit. It modulates a RF signal between 35 and 40 GHz with 16th harmonic of an LO frequency between 2 to 3 GHz. With an LO power of 17 dBm the mixer exhibits 35 dB conversion loss. Both RF and IF return losses are better than 10 dB. The chip size is 1 mm x 2.5 mm. A detailed description this mixer is presented in [8].

As shown in Fig. 6, the power amplifier in the transmit chain provides necessary output power. This three stage amplifier utilizes 1.6 mm output periphery and provides 16 +/- 1 dB gain with 23 dBm output power at 1 dB compression. The design approach is similar to that presented earlier in [9]. A detector has been added to the output stage of this power amplifier to provide easy monitoring of the output power level.



(a)



(b)

Fig. 6 Power amplifier (a) layout, (b) measured gain, input and output return loss as a function of frequency.

This HEMT diode detector has differential outputs to provide good tracking over temperature. The detector sensitivity is -0.95 mv/dB at -5 dBm level has a dynamic range from -10 dBm to 13 dBm. Power consumption is 620 mA when biased at 4 volts. The chip size is 5.0 mm x 2.5 mm.

The required performance of this chipset was achieved in first-pass. Several production lots of this chipset are currently in fabrication.

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